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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,482	09/27/2004	Pieter Jan Van Der Zaag	GB02 0030 US	5415

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,482	VAN DER ZAAG ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. **Status:** Receipt is acknowledged of papers submitted on February 16, 2007 under amendments, which have been placed of record in the file. Claims 1-16 are pending in this action. The amendment does not introduces any new matter into the disclosure. The added material, which is supported by the original disclosure. Please all the replies and correspondence should be addressed to examiner's new art unit 2629.

Applicant has amended abstract per objection, therefore objection to abstract is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daughton et al. (US 6,538,921 B1) as applied to claims 1 and 2 above, and further in view of Sharma (US 2003/0122790 A1).

Regarding Claim 1, Daughton et al. teaches a memory circuit (Col. 5, Lines 55) comprising: one or more magnetoresistive random access memories (page 6, Lines 31-34), MRAMs (Col. 6, Lines 31-40), coupled to a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

However, Daughton et al. one or more magnetoresistive random access memories , MRAM, a switching device; a pixel electrode; at least two MRAMs; and a bit line, the bit line running from the switching device to the pixel electrode; the bit line being arranged to cross over a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction.

However, Sharma teaches a memory circuit (page 2, paragraph 14, Lines 1-4)) comprising: one or more magnetoresistive random access memories, MRAM (page 4, paragraph 48, Line 1) a switching device (page 4, paragraph 48, Line 4) ; a pixel electrode (page 4, paragraph 48, Line 5); at least two MRAMs (page 5, paragraph 55, Lines 3,4); and a bit line (page 3, paragraph 35, Line 3), the bit line running from the switching device to the pixel electrode (page page 5, paragraph 54, paragraph 55, Lines 1-8); the bit line being arranged to cross over a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction (page 5, paragraph 55, see figure 12).

The reason to combine Daughton et al. teaches such memories can be advantageously based on the storage of digital symbols as alternative states of magnetization in magnetic materials provided in each memory storage cell, the result being memories which use less electrical power and do not lose information upon removals of such electrical power a memory circuit comprising: magnetoresistive random access memories MRAMs, but fails to teach a specific application such as display where a pixel structure of display is associated with MRAM where power consumption is major concerned.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Sharma to the teaching of Daughton et al. to be able to have a display system where a pixel structure of display is associated with MRAM which use less electrical power and do not lose information upon removals of such electrical power.

Regarding Claim 2, Daughton et al. teaches two MRAMs and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective one of the flip-flop circuit inputs (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

Claim 3, Sherma teaches each pixel is being associated with a respective one of the memory circuit (page 4, paragraph 48).

Claim 4, Daughton et al. teaches a memory circuit (Col. 5, Lines 55) comprising: one or more magnetoresistive random access memories (page 6, Lines 31-34), MRAMs (Col. 6, Lines 31-40), coupled to a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

However, Daughton et al. one or more magnetoresistive random access memories , MRAM, a switching device; a pixel electrode; at least two MRAMs; and a bit line, the bit line running from the switching device to the pixel electrode; the bit line being arranged to cross over

a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction.

However, Sharma teaches a pixel and memory assembly for a display device, comprising: a pixel display electrode coupled to in-pixel memory means, the in-pixel memory means comprising one or more MRAM (page 4, paragraph 48, page 5, paragraph 55) a memory circuit (page 2, paragraph 14, Lines 1-4)) comprising: one or more magnetoresistive random access memories, MRAM (page 4, paragraph 48, Line 1) a switching device (page 4, paragraph 48, Line 4) ; a pixel electrode (page 4, paragraph 48, Line 5); at least two MRAMs (page 5, paragraph 55, Lines 3,4); and a bit line (page 3, paragraph 35, Line 3), the bit line running from the switching device to the pixel electrode (page page 5, paragraph 54, paragraph 55, Lines 1-8); the bit line being arranged to cross over a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction (page 5, paragraph 55, see figure 12).

The reason to combine Daughton et al. teaches such memories can be advantageously based on the storage of digital symbols as alternative states of magnetization in magnetic materials provided in each memory storage cell, the result being memories which use less electrical power and do not lose information upon removals of such electrical power a memory circuit comprising: magnetoresistive random access memories MRAMs, but fails to teach a specific application such as display where a pixel structure of display is associated with MRAM where power consumption is major concerned.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Sharma to the teaching of Daughton et al. to

be able to have a display system where a pixel structure of display is associated with MRAM which use less electrical power and do not lose information upon removals of such electrical power.

Claim 5, Sherma teaches the in-pixel memory means further comprises a flip-flop circuit, the one or more MRAMs being coupled to the flip-flop circuit (page 4, paragraph 48, see figure 12).

Daughton et al. teaches a memory circuit (Col. 5, Lines 55) comprising: one or more magnetoresistive random access memories (page 6, Lines 31-34), MRAMs (Col. 6, Lines 31-40), coupled to a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

Claim 6, Daughton's teaches two MRAMs (item # 21 figure 10, Col. 23, Lines 55-58 where shows typical MRAM structure connected to flip-flop) and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective one of the flip-flop circuit inputs (item # 21 figure 10, Col. 23, Lines 55-58 where shows typical MRAM structure connected to flip-flop formed by nand gates 62,64 and detail of connection through several switching transistor to flip-flop and two MRAM cells item #21 figure 10 is described in detail Col. 23, line 65 to Col. 24, Line 32).

Claim 7, Sherma teaches a pixel and in-pixel memory for a display device (page 4, paragraph 48), comprising: a switching device; a pixel electrode; a first MRAM; a second MRAM (page 4, paragraph 48, page 5, paragraph 55) and a bit line (page 3, paragraph 35, Line 3), the bit line running from the switching device to the pixel electrode (page page 5, paragraph 54, paragraph 55, Lines 1-8); the bit line being arranged to cross over a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction (page 5, paragraph 55, see figure 12).

Daughton's teaches the bit line being arranged to cross over the first MRAM in a first direction and to cross over the second MRAM in a second direction, the first direction being substantially opposed to the second direction (please see figure 2, Col. 6, Lines Lines 31-40, teaches bit structure of two memory cells of MRAM and interconnection per claimed limitations also see figure 8B, Col. 21, Lines 32-47).

Claim 8, Daughton teaches routing bit lines of two memory cells connected in the series (see figure 8B) the bit lines is laid out such that it passes over the first MRAM 21 then turn or meanders back on itself before passing over the second MRAM 21 (Col. 21, Lines 32-47). Figure 10 also shows how two memory cells are connected in series to read or write data in magnetic memory cells. Daughton's prior art does suggests and discloses overall connection of the bit connection in series with driving circuitry (see Col. 5, Lines 50-60 which is similar to applicant's specification paragraph 10 of US PGPUB 2005/0116261 A1).

Sherma teaches the bit line being arranged to cross over a first MRAM in a first direction and to cross over a second MRAM in a second direction, the first direction being substantially opposed to the second direction (page 5, paragraph 55, see figure 12).

Claim 9, Sherma teaches a pixel and in-pixel memory for a display device comprising: a switching device; a pixel electrode (page 4, paragraph 48); a first MRAM; a second MRAM (see figure 12, page 5, paragraph 55); and further comprising: a word line (see figure 3, page 3, paragraph 35), running under the other ends of each of the first and second MRAMs, for addressing the MRAMs (See figures 8,3,12, page 4, paragraph 48, page 5, paragraph 55, page 3, paragraph 35) ; and a gate line, for driving the switching device, coupled to the switching device (page 4, paragraph 48); the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line (See figure 3,8,page 4, paragraph 48, page 3, paragraph 35, X11 bit line, X12 word line).

Claim 10, Sharma teaches a pixel and in-pixel memory for a display device (page 4, paragraph 48), comprising: a pixel display electrode coupled to in-pixel memory means, the in-pixel memory means comprising one or more MRAM (page 4, paragraph 48, page 5, paragraph 55) a memory circuit (page 2, paragraph 14, Lines 1-4) comprising: one or more magnetoresistive random access memories, MRAM (page 4, paragraph 48, Line 1) a switching device (page 4, paragraph 48, Line 4) ; a pixel electrode (page 4, paragraph 48, Line 5); at least two MRAMs (page 5, paragraph 55, Lines 3,4); and a bit line (page 3, paragraph 35, Line 3), the

bit line running from the switching device to the pixel electrode (page page 5, paragraph 54, paragraph 55, Lines 1-8); a word line, running under the other ends of each of the one or more MRAMs, for addressing the MRAMs (see figure 8, page 4, paragraphs 47,48 X12 word Line); and a gate line, for driving the switching device, coupled to the switching device (see figure 8, paragraph 48); the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line (see figures 8,3,12, page 3, paragraph 35, page 4, paragraphs 47,48, page 5, paragraph 55).

Daughton's teaches the bit line being arranged to cross over the first MRAM in a first direction and to cross over the second MRAM in a second direction, the first direction being substantially opposed to the second direction (please see figure 2, Col. 6, Lines Lines 31-40, teaches bit structure of two memory cells of MRAM and interconnection per claimed limitations also see figure 8B, Col. 21, Lines 32-47).

Claim 11, Sherma teaches a display device comprising a pixel and in-pixel memory (page 4, paragraph 48).

Claim 12, Sherma teaches the pixel and in-pixel memory (page 4, paragraph 48) is integrated with active matrix elements and drive lines of the display device (page 4, paragraph 46).

4. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma (US 2003/0122790 A1) in view of Matsuoka et al. (US 6,560,135 B2).

Claim 13 Sherma teaches a method of forming an in-pixel memory display device (page 4, paragraph 48), comprising: forming a switching device; forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit (page 4, paragraph 48, page 5, paragraph 55); forming a word line, for addressing the in-pixel memory circuit (page 3, paragraph 34,35, page 4, paragraph 47,48)), and forming a gate line, for driving the switching device (page 4, paragraph 48, page 5, paragraph 55).

However, Sharma fails to disclose the word line and the gate line are formed during a same masking stage.

However, Matsuoka et al. discloses the word line and the gate line are formed during a same masking stage (Col. 5, Line 63 to Col. 6, Line 35).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Sharma to the teaching of. Matsuoka et al. to be able to have a display system where a pixel structure of display is associated with MRAM where word line and bit line separated so the short does not occur which produces very stable writing in MRAM.

Claim 14, Sherma teaches a method of forming an in-pixel memory display device (page 4, paragraph 48), comprising: forming a switching device (page 4, paragraph 48, page 5, paragraph 55); forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit (page 4, paragraphs 46-48, page 5, paragraphs 54,55); forming a bit line, for addressing the in-pixel memory circuit (please see figure 8, page 4, paragraphs 46-48); forming a column line, for driving the switching device (see figure 8, page 4, paragraph 46-48).

. Matsuoka et al. the bit line and the column line are formed during a same masking stage (Col. 8, Lines 4-11 see figure 6).

Claim 15, Sherma teaches forming a word line, for addressing the in-pixel memory circuit (page 3, paragraph 34,35, page 4, paragraph 47,48), and forming a gate line, for driving the switching device (page 4, paragraph 48, page 5, paragraph 55)..

Matsuoka et al. discloses the word line and the gate line are formed during a same masking stage (Col. 5, Line 63 to Col. 6, Line 35).

Claim 16, Sherma teaches the in-pixel memory means further comprises a flip-flop circuit, the one or more MRAMs being coupled to the flip-flop circuit (page 4, paragraph 48, see figure 12).

Daughton et al. teaches a memory circuit (Col. 5, Lines 55) comprising: one or more magnetoresistive random access memories (page 6, Lines 31-34), MRAMs (Col. 6, Lines 31-40),

coupled to a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Perner et al. (US 6188615 B1) MRAM device including digital sense amplifiers.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

7. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

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Washington, D.C. 20231

Prabodh Dharia

Partial Signatory Authority Program

AU 2629

March 27, 2007